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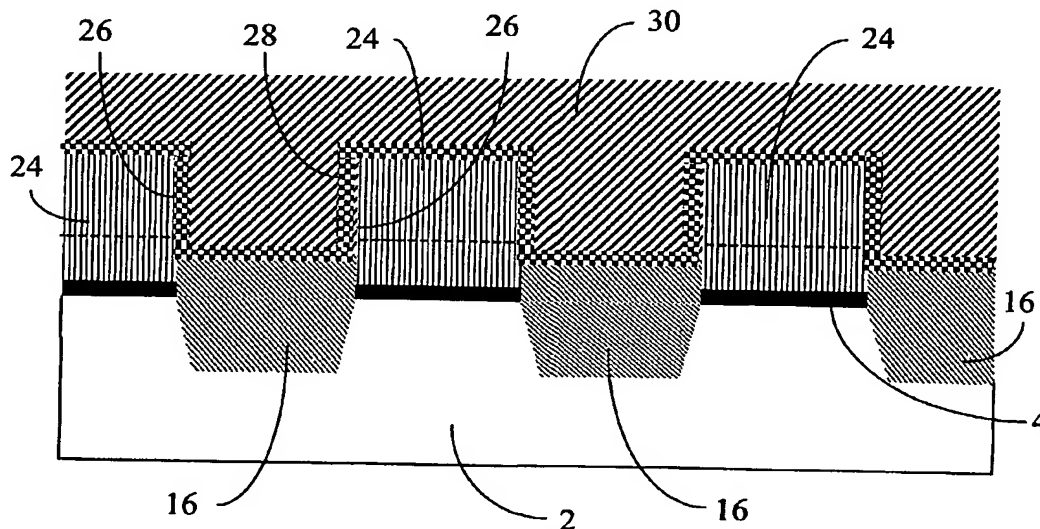
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- (71) Applicant (for all designated States except US): **KONINKLIJKE PHILIPS ELECTRONICS N.V.** [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).
- (72) Inventors; and
- (75) Inventors/Applicants (for US only): **VAN SCHAIJK, Robertus, T., F.** [NL/NL]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL). **VAN DUUREN, Michiel, J.** [NL/BE]; c/o Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).
- (74) Agent: **GROENENDAAL, Antonius, W., M.**; Philips Intellectual Property & Standards, Prof. Holstlaan 6, NL-5656 AA Eindhoven (NL).
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(54) Title: SHALLOW TRENCH ISOLATION IN FLOATING GATE DEVICES



(57) Abstract: The present invention provides a method for manufacturing a floating gate type semiconductor device on a substrate having a surface (2), and a device thus manufactured. The method comprises: - forming, on the substrate surface, a stack comprising an insulating film (4), a first layer of floating gate material (6) and a layer of sacrificial material (8), - forming at least one isolation zone (18) through the stack and into the substrate (2), the first layer of floating gate material (6) thereby having a top surface and side walls (26), - removing the sacrificial material (8), thus leaving a cavity (20) defined by the isolation zones (18) and the top surface of the first layer of floating gate material (6), and filling the cavity (20) with a second layer of floating gate material (22), the first layer of floating gate material (6) and the second layer of floating gate material (22) thus forming together a floating-gate (24).

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## A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H01L27/115 H01L21/8247

According to International Patent Classification (IPC) or to both national classification and IPC

## B. FIELDS SEARCHED

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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal

## C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US 6 391 722 B1 (KOH CHAO-MING) 21 May 2002 (2002-05-21) the whole document	1,2,4, 6-10
X	US 6 222 225 B1 (ARAI FUMITAKA ET AL) 24 April 2001 (2001-04-24) column 5, line 6 - column 6, line 16; figures 5a-5h	1-4,6, 8-10
X	US 2002/093073 A1 (NOGUCHI MITSUHIRO ET AL) 18 July 2002 (2002-07-18) paragraph '0051! - paragraph '0059!; figures 3a-4c	1,4,6, 8-10

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Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2  
NL - 2280 HV Rijswijk  
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,  
Fax: (+31-70) 340-3016

Authorized officer

Baillet, B

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